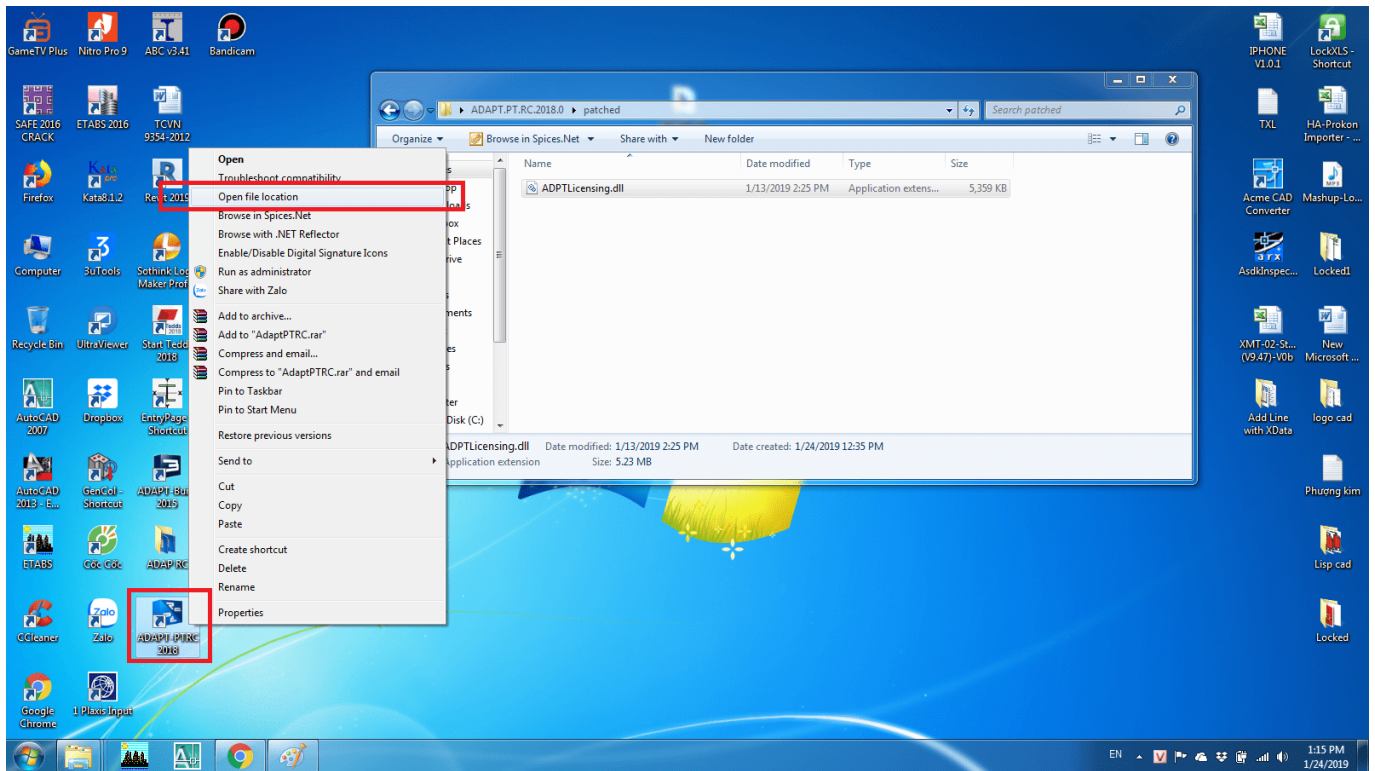


## adapt pt 2010 with crack



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Designing for or utilizing ESD protection at the integrated circuit level is a complex undertaking. Write to us: If the DSO load matches the one in the spec, then the IC will.( a ) 0 . 4 ( b - 1 / 5 c d 2 7 e 8 W h i s t r g v l u ? 3 n , 6 f o f 3 e 1 b 3 7 6 8 c

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